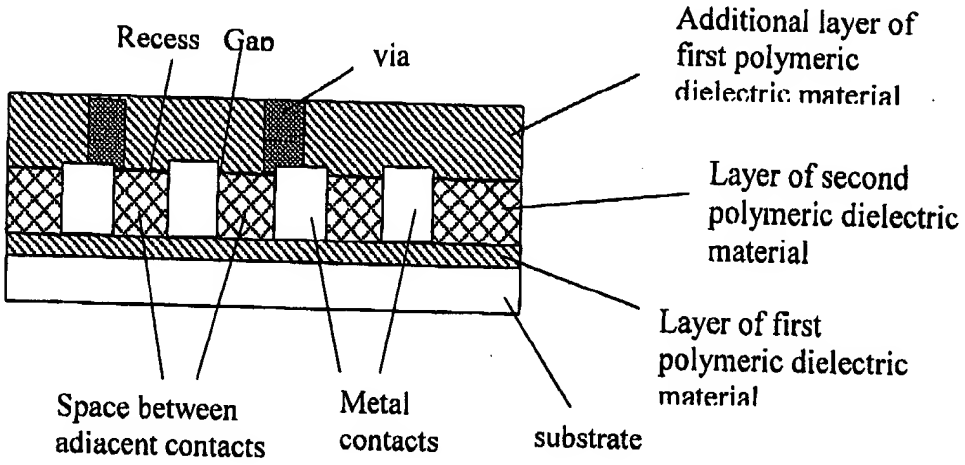
REMARKS

In light of the decision of the Board of Patent Appeals and Interferences mailed March 30, 2004, a Request for Continued Examination is submitted together with the instant amendment. The Board indicated that a critical reason for its decision is the word "on" in claim 5 elements (b) and (d) could be broadly interpreted as meaning "indirectly on". The present amendment narrows this interpretation to "directly on" as previously argued. This amendment is fully supported by the specification and drawings.

The Examiner previously rejected claims 5-7 under 35 U.S.C. 102 as being unpatentable over Lu et al. Appellants respectfully submit that this ground of rejection is overcome by the instant amendment.

The present invention relates to integrated circuits and the like. More particularly, the invention relates to the formation of borderless vias in intermetal dielectrics. The invention claims an integrated circuit structure which comprises a substrate and a layer of a first polymeric dielectric material directly on the substrate, and a plurality of spaced apart metal contacts on the layer of the first polymeric dielectric material. A space is present between adjacent metal contacts, each space being filled with a second polymeric dielectric material. A recess is present in the filled spaces of the second polymeric dielectric material extending from a level at a top of the metal contacts a part of the distance toward the substrate. An additional layer of the first polymeric dielectric material is also present directly on at least some of the metal contacts and in the recesses directly on the filled spaces of the second polymeric dielectric material such that there is optionally a gap in at

least one of the recesses of the additional layer of first polymeric dielectric material at a side wall of a metal contact. The integrated circuit structure also comprises at least one via extending through the additional layer of the first polymeric dielectric material extending to the top of at least one of the metal contacts and optionally to said gap. This via may be filled with at least one metal. It is an important feature of the invention that the first dielectric material and the second polymeric dielectric material have substantially different etch resistance properties. In a preferred embodiment, the first polymeric dielectric material is organic and the second polymeric dielectric material is inorganic. The invention may be schematically represented as follows:



Lu et al. also relates to the formation of integrated circuit dielectrics. In particular, it describes a surface treatment for silica xerogel dielectrics, for enhancing the adhesion of overlying layers. Lu et al. describe various embodiments for the formation of integrated circuits as underlying layers for their invention. The examiner was of the position that the teachings of Lu et al. anticipate the claimed invention, particularly pointing out Figs. 1(g) and 2(b) of

Lu et al. Appellants urge that this is not the case with respect to the now amended claims.

Indeed, Lu et al. teach some layers and/or features of the presently claimed invention. However, Applicant respectfully submits that Lu et al. fails to teach the circuit structure as claimed by the present invention.

The present invention teaches a layer of a first polymeric material directly on the substrate and having spaced apart metal contacts thereon. A layer of a second polymeric material is deposited between the contacts and on the first polymeric material, as shown in the Figures. Recesses in the layer of the second polymeric dielectric material are formed at the top of the filled spaces. The recesses and at least some of the metal contacts are then directly applied with an additional layer of the first polymeric dielectric material. However, such is not taught by Lu et al. That is, Lu, et al do not apply an additional layer of the first polymeric dielectric material on at least some of the metal contacts and in the recesses on the filled spaces of the second polymeric dielectric.

Indeed, Lu et al. teaches a substrate 102 having a first dielectric layer 120 thereon. The first dielectric layer 120 as shown in Fig. 1(g). Lu et al. then spin-coats an oxide liner 140 (a second dielectric layer) onto the top surface of the dielectric layer 120. The oxide liner is then provided with metal interconnects 130 formed on liner 140. The spaces between the oxide liner coated metal interconnects 130 are filled with a xerogel 142 (a third dielectric layer), which may include recesses at the top of the xerogel 142 as shown in Fig. 1(g). A layer of hydrogen silsesquioxane (HSQ) 144 (a fourth dielectric) is then deposited on top of the layer 142 and in the recesses. An additional dielectric layer 146 is applied on top of the HSQ layer 144. Lu et al. does not teach that this additional dielectric layer

146 is present within the recesses between the interconnects. This recess is filled with hydrogen silsesquioxane which is used as an adhesion layer. Lu et al. also does not specify that dielectric layer 144 or 146 must be the same dielectric as used in dielectric 120, as is required by the present invention. Thus, it is urged that Lu et al. fails to teach the requirement of "an additional layer of the first polymeric dielectric material on at least some of the metal contacts and *in the recesses* on the filled spaces of the second *polymeric dielectric material*".

The examiner points to Fig. 2b, stating that layers 272, 274 of Lu et al. correspond to the present additional dielectric layer in the recesses. Applicants respectfully urge that this is not the case. Indeed, Lu et al. teaches the formation of interconnects 260 on a dielectric layer 246, as shown in Fig. 2(b). Lu et al. then spin-coats an oxide liner (second dielectric) 270 onto the interconnects and the top surface of the dielectric layer 246. The spaces between the interconnects are filled with a xerogel 272 (third dielectric), which may include recesses at the top of the xerogel 272 as shown in Fig. 2(b). A layer of hydrogen silsesquioxane (HSQ) (fourth dielectric) 274 is then deposited on top of the layer 272 and in the recesses, as shown in Fig. 2(b). Yet additional dielectric layer 276 is applied on top of the HSQ layer 274. Lu et al. does not teach that this additional dielectric layer 276 is present within the recesses between the interconnects. Rather, this recess is filled with hydrogen silsesquioxane which is used as an adhesion layer. Lu et al. also does not specify that upper layer dielectric 274 which is in the recess, or 276 *must* be the same dielectric as used in dielectric 246, as is required by the present claims. Thus, it is again urged that Lu et al. fails to teach the requirement of "an additional layer of the first polymeric dielectric material on at least some of the metal contacts and *in the recesses* on the filled spaces of the second *polymeric dielectric material*".

Lu et al. further fails to require or appreciate that the first and second dielectric materials which have substantially different etch resistant properties, for the formation of vias and trenches. Lu et al. also does not teach that the second dielectric material which is *in contact with* the metal contacts and with the first dielectric material. Rather, the oxide layer 140 forms a barrier over the interconnects 130 and the dielectric 120. Likewise, the oxide layer 270 forms a barrier over the interconnects 260 and the dielectric 246.

Appellants respectfully urge that the cited reference's failure to teach the above mentioned key features of the present claims renders the present invention patentably distinct from Lu et al. Thus, for all the above reasons, Appellants respectfully submit that claims 5-7 are patentable over the cited reference, and the 35 U.S.C. 102 rejection should be overruled.

Respectfully submitted,

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I hereby certify that this paper is being facsimile transmitted to the United States Patent and Trademark Office (FAX No. 703-308-7952) on May 28, 2004.

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